IBIN-A, IBIN-LP PC Interfaces

The IBIN-A interface plugs into any slot in an IBM PC/XT/AT/386/486 Personal System/2 Models 25, 30, or compatible, and serves as an interface between the computer and the Series 500. In addition, the interface card hosts other functions common to the Series 500 system: the programmable interval timer, and the switch selectable wait state generator.

The IBIN-LP is a low-power version of the standard IBIN-A interface which was designed for use in lap-tops or other computers which cannot supply enough current in their expansion slots to power the standard IBIN-A. The IBIN-LP achieves its reduced power requirement through the use of low-power components. Physically, the IBIN-A and IBIN-LP are identical, and share the same component layout and designations. Instructions for installation and use are also the same for both cards.

The programmable interval timer can be used to time events, create software delays, and generate periodic interrupts in the PC. The timer consists of three independent 16-bit counters with a resolution of one microsecond. The three counters can be cascaded to create longer timing intervals.

The wait state generator provides compatibility with many computers which use non-standard bus timing or processor speeds.

Configuring the IBIN-A Interface Card

User configurable features of the IBIN-A interface include an address mapping switch, a PC bus wait state generator switch, and a removable cable for connecting the interface card to the Series 500 system. In addition, there are several jumpers that can be used in special applications to achieve additional flexibility.

Switch S1 selects the address range of the interface in the system memory map. This switch is normally set for a starting location of hex CFF80 (the factory default), but can be configured over the full one megabyte addressing range of the PC. The switch setting determines the most significant 8 bits of the Series 500's address region, which is 4K in size. The upper 128 bytes of memory in this 4K area contain the active memory locations used to communicate with the Series 500.

Functionally, switch set S1 consists of two groups of four switches. Switches 1-4 control which 64K segment of memory the IBIN-A resides in. For any 64K segment, the second address digit can be set from 0 through F (hex). The last three digits of the address are hard-wired to "F80". This permits the interface address to be set to the top 127 bytes of consecutive 4K blocks of memory within any 64K segment.

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Table 1. IBIN-A Address Switch Setting Information

64K Segment	1	2	3	4	4K Region	5	6	7	8
Fxxxx	off	off	off	off	xFF80	off	off	off	off
Exxxx	off	off	off	on	xEF80	off	off	off	on
Dxxxx	off	off	on	off	xDF80	off	off	on	off
Cxxxx	off	off	on	on	xCF80	off	off	on	on
Bxxxx	off	on	off	off	xBF80	off	on	off	off
Axxxx	off	on	off	on	xAF80	off	on	off	on
9xxxx	off	on	on	off	x9F80	off	on	on	off
8xxxx	off	on	on	on	x8F80	off	on	on	on

As an example, to set the interface to respond at address CFF80 you would set the switches 1 through 8 as follows:

1	2	3	4	5	6	7	8
off	off	on	on	off	off	off	off

An address range which is almost universally available regardless of computer is CAF80 through CFF80. Note that many of the possible addresses will conflict with other hardware, RAM, or ROM already in the computer, so the practical range of addresses is fewer than the switches provided for. However, there will normally be many more addresses available than are actually needed.

Hardware options for the PC or AT, such as fixed disks, enhanced graphics adapters, and expanded memory occupy portions of the PC memory map, and preclude using the same addresses for the IBIN-A interface. Memory conflicts occur when the computer attempts to read an address occupied by more than one piece of hardware. These problems can be manifest as error messages at boot-up, or failure of the computer or data acquisition system to operate properly. If this occurs, examine the memory usage of all hardware in your computer, and make changes where necessary. Usually, changing the address of the IBIN-A interface is all that is required.

The following is a map of common memory usage in a standard AT or 386:

F0000-FFFFF: Universally used for ROM BIO5. Interface should generally not be addressed to this block.

E0000-EFFFF: Used by some 16 bit VGA cards. May be used by Lotus-Intel-Microsoft "EMS" expansion memory. Also reserved for system use in AT-class computers. If no functions or hardware use all these addresses, area may be used for IBIN-A interface.

D0000-DFFFF: May be used by Lotus-Intel-Microsoft "EMS" expansion memory. This page is often the location of a LAN card. If no functions or hardware use all these addresses, area may be used for IBIN-A interface.

C0000-CFFFF: Lower portion of this page typically occupied by Fixed disk ROM BIO5 and Video BIO5 ROM. Interface can be set to use CAF80 through CFF80 for most systems.

A0000-BFFFF: Universally used by VGA, EGA, or CGA. Interface cannot be set to this block. This area not normally available for interface.

00000-9FFFF: RAM space from 0K to 640K. This area should not be used for interface.

You should have no technical difficulty finding usable addresses, although you may have to do some research to find out what addresses are free in your computer. Normally, CFF80 will be compatible with any computer and installed hardware.

Memory Conflicts

In very rare cases, a system may be loaded with options which use addresses in the C000, D000, and E000 address blocks. Increasingly, hardware and software options such as EMS memory, "shadowed ROM BIOS", and VGA cards are being added by computer manufacturers or end users. These options can monopolize the one or two complete pages of memory. If the C000, D000, and E000 pages are all used, the process of integrating the computer and IBIN-A becomes much more complex. Finding a free address in such computers can require trial and error testing, a search through the computer documentation, or a call to the computer manufacturer. The IBIN-A installation may ultimately result in a sacrifice of some of the computer's speed, enhancements, or overall performance. Examples include:

1. 16-BIT VGA VIDEO ADAPTERS — Some VGA adapters feature 16-bit addressing, and use addresses up to E000:0. These cards can be identified by the presence of a second AT-type card edge connector behind the main card-edge connector. Memory usage will vary as the adapter enters and leaves its various display modes. When the card permits, the solution is to reconfigure the VGA for 8-bit operation by setting switches or running utility software. This may cause a reduction in video update speed or loss of some unique resolution modes or enhancements designed in by the VGA manufacturer.
2. EMS MEMORY — Expanded memory is also called "paged" memory. EMS was originally designed to provide PC/XT computers with up to eight or more megabytes of RAM, even though the 8088μP can address only 1 Mbyte of memory. EMS can also be used in 286- and 386-based computers. Most EMS boards require a free, contiguous 64k address space which acts as a window into all the EMS memory. The solution is to install the EMS software to specifically exclude the space that the IBIN-A requires. Instructions for excluding a particular range of segment addresses for an EMS page are given below for three popular 386 expanded memory manager packages. Add the exclude statement to the CONFIG.SYS declaration which corresponds to the memory manager you are using.

386 Expanded Memory Manager	Exclude Statement	CONFIG.SYS Declaration	Minimum Exclusion
DOS 5.0's EMM386	X = CF00-D000	DEVICE = EMM386.EXE	4K
Qualita's 386 MAX	EXCLUDE = CC00-D000	DEVICE = 386MAX.SYS	16K
Quarterdeck's QEMM	EXCLUDE = CF00-CFFF	DEVICE = QEMM.SYS	4K

Each of the above examples assumed that the IBIN-A address switch is set to the default CFF8 hex. Note: an exclude statement is required because the IBIN-A cannot be detected by a memory manager. A memory manager is likely to take all unexcluded memory blocks for its own use.

3. "SHADOWING" — This technique copies system ROM BIOS or VGA BIOS information stored in relatively slow system ROM chips to faster-reading RAM, usually in the D000 or E000 pages. Once in RAM, the information can be read more quickly by the computer's μP, resulting in a faster system. By itself, shadowing does not necessarily consume all the available high memory addresses. However; a system which combines shadowing, 16-bit VGA, and EMS memory may leave no addresses vacant for the IBIN-A. Consult your computer documentation for instructions on disabling the shadow RAM.

Any of these problems require a careful study of the documentation for the affected hardware to determine how memory is allocated in a specific computer, and what steps may be available to solve the problem. Keithley can offer specific suggestions on setting up the IBIN interface, but users may have to contact vendors of the other equipment to find a complete solution.

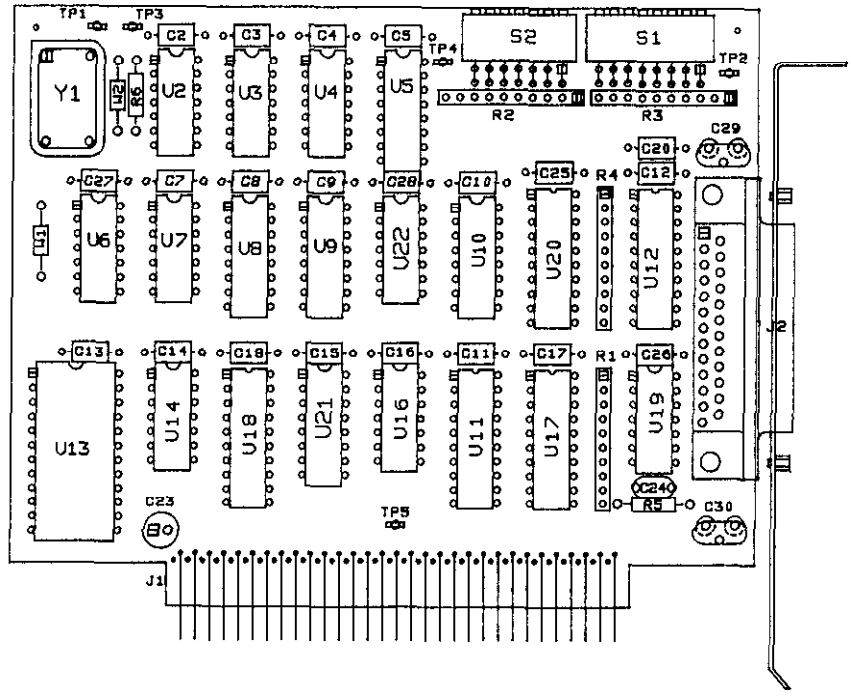


Figure 1. IBIN-A Interface

See Table 2 for user-configured components on the interface card. See Figure 1 for an illustration of the PC interface.

Table 2. User-Configured Components on the IBIN-A

Name	Designation	Function	Default
Cable 1	*CB1*	*Cable between IBIN-A and Series 500.*	—
Switch set S1	S1	Memory Address Range Switch	CFF80
Switch set S2	S2	Wait State Selector Switch	disabled
Jumper W1	W1	External Interrupt Enable/Disable	installed
Jumper W2	W2	Series 500 Interrupt Enable/Disable	removed
EXT INT	TP1	External Interrupt Connect (used with W1)	—

Installing the IBIN-A Interface Card

CAUTION: Turn off the power before installing or removing the interface card in the computer.

The IBIN-A interface is installed into expansion slots inside the PC system unit. It may be installed into any vacant slot of the computer.

Install the IBIN-A into an expansion slot as follows: Make sure the PC is turned off, and unplug the power cord. Consult the computer manufacturer's documentation for instructions on opening the computer. Remove the outer case and any other covers to gain access to the computer's expansion slots.

A rear panel opening is provided at the end of each expansion slot for mounting I/O connectors. If a slot is unused, then this opening will be covered by a metal plate held in place by a screw on top of the plate. Remove the retaining screw and cover plate from the desired expansion slot. **Be very careful not to drop the retaining screw into the computer, it may be difficult to retrieve.**

Carefully insert the IBIN-A into the expansion slot, fitting the DB25 connector through the rear panel operating so that the mounting bracket is in the correct position to be fastened securely by the retaining screw removed earlier. Insert the card edge into the mother board card edge receptacle. With the board firmly in place, install and tighten the retaining screw. Finally, attach the interfacing cable to the connector (J2) on the interface card at the rear of the computer. The cable connecting the PC to the Series 500 is a shielded 23-contact cable. The cable should be attached to the baseboard of the Series 500 unit. Never strain the connection between cable and connector. The outer end of the cable should be plugged into the connector (J117) on the rear panel of the Series 500 base unit. This connection should be made with power to the Series 500 turned off. Avoid entangling the interface cable in 60 cycle AC power lines.

Software Installation and Wait States

Switch SW2 enables and disables the wait state generator. For most computers, this feature can be left disabled (all wait state switches set to OFF). The need to change the wait state switches will become evident for a given computer if certain problems arise during installation or operation of software. For instance, some PC compatibles running at rates higher than 8MHz will not work properly with the Series 500. One indication would be if the INSTALL program supplied with KDAC500 aborts or issues error messages such as "Interface not found" or "Can't trigger interrupts". Another indication would be if KDAC500 installs correctly, but later yields incorrect data during acquisition.

If you are running a compatible computer which uses non-standard bus or processor speeds, you should try installing KDAC500 even if you are planning to use a software package other than KDAC500. If any timing problems exist, you may then add wait states to see if the problem can be corrected.

To change the number of wait states, see Figure 1 to locate switch S2. There are seven switches on the S2 switch set. In order to add one wait state to the bus you would set switch 1 to on. Re-install the Keithley software, and then re-run your test. If the system still does not function, try setting both 1 and 2 on. Continue in this manner until all switches are on. Run the INSTALL software supplied with the Keithley software each time you make a change.

If you are using a third-party software package, consult its documentation for installation details.

Interrupt Selection

The interrupt levels, in order of priority, are shown in the following chart. Interrupt usage is controlled through software;

PC or XT (8088 or 8086)	AT (80286) or 80386
CLOCK	CLOCK
LEV2	LEV9
LEV3	LEV3
LEV5	LEV5

See the installation section of the KDAC500 software manual for complete instructions on running INSTALL with command modifiers which select other interrupts.

Jumper Settings for Selection of Interrupt Source

Method of Interrupt Generation	Jumper W1	Jumper W2	Note:
On board timer 8254 (Default)	Installed	Removed	Default
External interrupt applied to TP1	Removed	Removed	Allows synchronization to an external time base.
Interrupt generated by a Series 500 option module	Removed	Installed	500-TRG1 is currently the only module which can generate an interrupt.

Hardware installation is completed. Reassemble the computer in reverse order of disassembly, being careful that no screws or other hardware have dropped into the system. Plug the computer's power cord back in.

Interrupt Conflicts

The IBIN-A interface can use the NMI (Non-Maskable Interrupt), CLOCK, INT2, INT3, or INT5 for interrupt-driven data acquisition under Keithley's KDAC500 software. The selection is made during the installation of the software, with NMI being the default. The interrupts are activated by the CALL INTON command. Third-party software packages can have their own interrupt strategies, but quite often use CLOCK.

Keithley recommends using the NMI because the NMI takes priority over all other system interrupts and events, and gives the most precisely-timed acquisition. The NMI was originally designed for use with memory parity checking. However, some hardware accessories also use the NMI for other tasks. Among these are "auto-switching" EGA cards and the dynamic RAM refresh of some Zenith comput-

ers. Such systems will operate properly until the user runs a data acquisition program including a CALL INTON command, at which point a "Parity Check" or other error results.

There are two solutions to making the IBIN-A work in systems which use the NMI for other functions. One is to disable the other hardware's use of the NMI. Some EGA cards have a switch or programmable register to disable use of the NMI. This is not possible with all hardware, and the second solution is to simply install the Keithley software to use another of the available IBIN-A interrupts.

Interrupt Usage in PCs and ATs

Keithley's KDAC500 can be installed to use the NMI, CLOCK, INT2, INT3, or INT5 interrupts. The actual choice of interrupt depends on other hardware which may be in the system.

The following table summarizes interrupt usage in XT-type computers:

INT	Application
0	Timer
1	Keyboard
2	Reserved
3	Secondary asynch adapter (COM2)
4	Primary asynch adapter (COM1)
5	Hard disk controller
6	Floppy disk controller
7	Printer (not used in most machines)

The following rules can be defined for XT computers:

1. Use NMI for the most precisely timed data acquisition.
2. If NMI causes problems in the system, consider INT2, INT3, or INT5 in that order.
3. If the XT contains a hard disk, INT5 cannot be used.
4. If the system contains COM1 and COM2, INT3 cannot be used. A serial mouse and an available COM port probably eliminate INT3. A bus mouse and one COM port may leave INT3 available. A LAN adapter probably uses INT3.
5. If there are no other adapter boards in the computer, INT2 is probably available, although some multi-function I/O boards may use INT2.
6. Use CLOCK as a last alternative.

The following table summarizes interrupt usage in PC/AT computers:

INT	Application
0	Timer
1	Keyboard
2	Orred summary of INT8-INT15
3	Secondary asynch adapter (COM2)
4	Primary asynch adapter (COM1)
5	Parallel port 2 (LPT2)
6	Floppy disk controller
7	Parallel port 1 (LPT1)

This table provides these guidelines for AT computers:

1. Use NMI for the most precisely timed data acquisition.
2. If using NMI causes problems in the computer, consider INT2, INT3, or INT5 in that order.
3. On a true AT compatible, INT2 is not available. However, many AT compatibles do not use INT2 as the original IBM PC/AT did. In this case, INT2 may be usable.
4. If the computer contains COM1 and COM2, INT3 cannot be used. A serial mouse and a COM port probably make INT3 unavailable. A bus mouse and a single COM port probably mean INT3 is available. A LAN adapter probably uses INT3.
5. If the computer contains no other adapter boards, then INT5 is probably available.
6. While INT5 is assigned for printer use, there seem to be few printer adapters that really use interrupts. In fact, the DOS print spooler does not support it. Therefore, INT5 is usually a workable alternative (provided something else doesn't use it).
7. Use CLOCK as a last alternative.

In summary, use NMI if possible. To use INT2, INT3, or INT5, first determine what other options may be using these interrupts and choose accordingly. The ultimate confirmation of whether a given interrupt is suitable may require trying it. The usual symptoms of interrupt conflicts are POST error messages, bad data, or a locked-up computer. Since INT2, INT3, and INT5 are used by various hardware options, problems with serial ports, fixed disks, or printer ports may also occur, although they have been rare. These symptoms will usually appear immediately when the system is turned on, or soon afterward. Use CLOCK as a last alternative.

Programmer Model for the Memory Map

A summary of memory locations used with the interface card is given in Table 3. These addresses correspond to the "Command A" and "Command B" functions which are associated with each module in the Series 500 module library. Note that some modules also use "Command C" and "Command D" ad-

dresses for special functions. Collectively, these addresses are labeled "CMDA", "CMDB", CMDC", and "CMDD".

Table 3. Memory Map Locations and Functions

Function/Use		Location
Slot 1	CMDA	xxx00
	CMDB	xxx01
	CMDC	xxx1A
	CMDD	xxx1B
Slot 2	CMDA	xxx02
	CMDB	xxx03
	CMDC	xxx18
Slot 3	CMDA	xxx04
	CMDB	xxx05
	CMDC	xxx19
Slot 4	CMDA	xxx06
	CMDB	xxx07
Slot 5	CMDA	xxx08
	CMDB	xxx09
Slot 6	CMDA	xxx0A
	CMDB	xxx0B
Slot 7	CMDA	xxx0C
	CMDB	xxx0D
Slot 8	CMDA	xxx0E
	CMDB	xxx0F
Slot 9	CMDA	xxx10
	CMDB	xxx11
Slot 10	CMDA	xxx12
	CMDB	xxx13
R/W COUNTER 0		xxx40
R/W COUNTER 1		xxx41
R/W COUNTER 2		xxx42
COUNTER CONTROL		xxx43
TIMER GLOBAL		xx60
TIMER STATUS		xxx61
CLEAR INTERRUPT		xxx62
SET INT LEVEL		xxx63

(Presumes prior execution of a DEF SEG=CFF8 command)

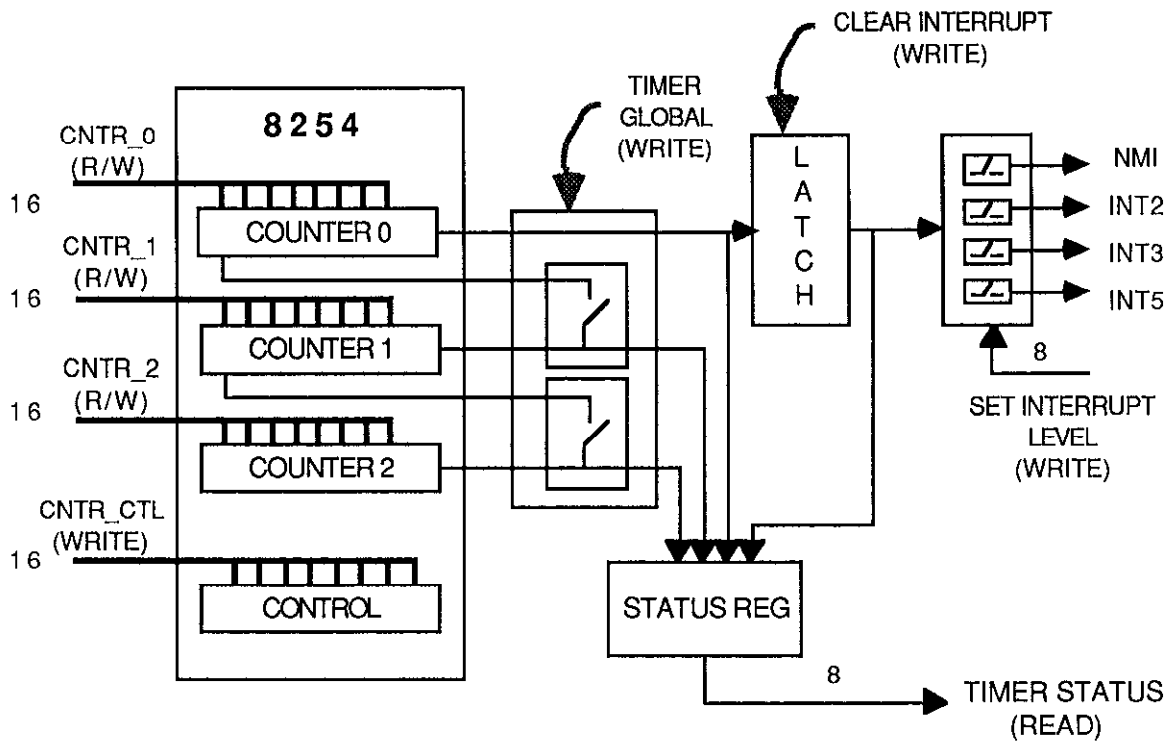


Figure 2. Functional Block Diagram of IBIN-A Timer Circuit

R/W COUNTER 0

Location: xxx40

This location is used to load counter 0 with the interval count, as well as to read the interval from that counter. Data to this location is always sent as two bytes in succession. The first WRITE (or READ) is the low byte of the count, and the second WRITE (or READ) the high byte. The read or write must be issued twice for the counter to function. The counter automatically makes the low byte register available first; and then responds to the second R/W command by making the high byte register available.

A write to COUNTER CONTROL (see discussion below) must always precede any R/W COUNTER commands.

R/W COUNTER 1

Location: xxx41

This location is used in the same way as R/W counter 0, except it applies to counter 1.

R/W COUNTER 2

Location: xxx42

This location is used in the same way as R/W COUNTER 0, except it applies to counter 2.

COUNTER CONTROL

Location: xxx43

An access to the COUNTER CONTROL location always prefaces the R/W COUNTER commands discussed above, indicating to the timer which of the three counters is to be addressed, and in what mode that counter will be used. COUNTER CONTROL should always be followed by two successive R/W COUNTER commands for the specified counter.

The counters can be used in three modes: interrupt generator, carry generator, and latch mode. Counter 0 cannot be used as a carry generator, and counters 1 and 2 cannot generate interrupts. This functionality is due to the TIMER GLOBAL circuitry discussed below.

The interrupt mode allows counter 0 to produce periodic interrupts. When two or three counters are linked, the carry generator mode causes the terminal count of one counter to trigger the count in another counter (see Table 4). The counters can be used simply for timing events and creating software delays by masking off the interrupts using the TIMER GLOBAL location.

Table 4. Values Written to COUNTER CONTROL

Mode	Counter 0	Counter 1	Counter 2
Interrupt Generator	00110100 Hex 34 52	Not used	Not used
Carry Generator	Not used	01110100 Hex 74 116	10110100 Hex B4 180
Latch	00000000 Hex 00 0	01000000 Hex 40 64	10000000 Hex 80 128

In general, the count is always carried from counter 2 to counter 1 to counter 0. When linked, counter 0 is always the carrier of counts generated by higher numbered counters, and should be set to interrupt mode. The higher numbered counters should be set to carry generator mode. When only counters 2 and 1 are linked, counter 1 should be set to interrupt mode, and counter 2 to carry generator mode.

The latch mode is used to read the counters. The latch transfers the count into an intermediate register, allowing a stable reading without distributing the count in progress. Table 5 describes the bit configuration of values written to the COUNTER CONTROL location.

Table 5. Bit Configuration of Values Written to COUNTER CONTROL

D7	D6	D5	D4	D3	D2	D1	D0
(----SC----)		(----W/L----)		0	1	0	0

Explanation:

SC (Select Counter)	Counter 0 - 00 Counter 1 = 01 Counter 2 = 10
W/L (Write/Latch)	Latch = 00 Write = 11

TIMER GLOBAL

Location:xxx60

This location is used to set mode of the timer circuitry. This command should be issued prior to the COUNTER CONTROL and R/W COUNTER commands. If it is not issued, all interrupt and carry functions will remain in their previous state.

The lower three bits of this location determine whether the interrupt circuitry of the timer is enabled, and whether any of the counters will be linked with the carry generator.

When the computer is first turned on or when the system is rebooted, interrupts are initialized to off and there are no cascaded counters.

Table 6 provides a summary of values written to the TIMER GLOBAL location. Table 7 describes the bit configuration of these values.

Table 6. Values Written to TIMER GLOBAL

Mode	No Carry	Carry 1-0	Carry 2-1	Carry 2-1-0
Counter 0 interrupt off.	0000 H00 0	0010 H01 1	0001 H02 2	0011 H03 3
Counter 0 interrupt on.	0100 H04 4	0101 H05 5	0110 H06 6	0111 H07 7

Table 7. Bit Configuration of Values Written to TIMER GLOBAL

D7	D6	D5	D4	D3	D2	D1	D0
INT	X	X	X	X	C2	C1	C0

Explanation:

X	Not used	
INT	Interrupt ON/OFF	(OFF = 9, ON =1)
2-1 Carry	Counter 2 - Counter 1	(OFF =0, ON = 1)
1-0 Carry	Counter 1 - Counter 0	(OFF = 0, ON =1)

TIMER STATUS

Location: xxx61

The TIMER STATUS location can be read to provide the output status of the interrupt circuitry and the three counters of the 8254 counter/timer. The status of the interrupt latch is assigned to bit 7, and the status of counters 0, 1 and 2 are assigned to bits 0, 1 and 2, respectively (see Table 8).

Table 8. Bit Configuration of Values Read from TIMER STATUS

D7	D6	D5	D4	D3	D2	D1	D0
INT	X	X	X	X	C2	C1	C0

Explanation:

X	Not used
INT Interrupt status	1 = Active interrupt 0 = No interrupt
C2 Counter 2 status	1 = Output line high 0 = Output line low
C1 Counter 1 status	1 = Output line high 0 = Output line low
C0 Counter 0 status	1 = Output line high 0 = Output line low

If there is more than one device generating interrupts in the system, the interrupt processing routine must determine whether the interrupt received was generated by the Series 500 unit. Each time the Series 500 generates an interrupt, bit 7 of the TIMER STATUS location is set to 1. This bit is cleared to 0 when the CLEAR INT command is issued.

The other bits in this location are used in software delay routines. Each of these bits is set independently, and can be read separately. When a counter is first loaded, the bit is set to 1. Halfway through the count, the bit is set to 0, and at the terminal count, the bit is reset to 1. A delay routine waiting for the terminal count should first check for 0, and when 0 has been read, check for 1.

CLEAR INTERRUPT

Location: xxx62

This location is used to clear the interrupt status bit of the timer status location to 0, and is used in interrupt processing routines to allow the generation of subsequent interrupts. It should be issued after saving the registers and assessing the source of the interrupt (see TIMER STATUS) but before other actions in the interrupt processing routine. If this command is not issued, no further interrupts will be generated by the Series 500 circuitry.

Writing any number to this location will clear the interrupt circuitry (0 is often used to convenience, but is not required).

SET INT LEVEL

Location: xxx63

This location is used to select the type of interrupt generated by Timer 0 when the interrupt mode is enabled. It should be issued as part of the set-up sequence for interrupt generation. The SET INT LEVEL location only needs to be setup once prior to interrupts being enabled.

For correct operation, only one interrupt level should be selected. To select a level, a 0 is placed in he corresponding bit position and a 1 placed in all other locations (see Table 9). Selecting more than one interrupt level will cause unpredictable results in interrupt processing. For more information on interrupt processing from the 8088 or 80286 processor, consult your PC and Intel technical publications.

Table 9. Bit Configuration of Values Written to SET INT LEVEL

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	NMI	L5	L3	L2

There are four types of interrupts which can be selected. "NMI" causes a non-maskable interrupt, and "L2", "L3", and "L5" refer to maskable interrupts with priority levels 2, 3, and 5 respectively.

Theory of Operation

The interface to the Series 500 is provided through connector J2. Control of the Series 500 is accomplished through address lines MBA0-MBA4, as well as MBR/W, and MBSEL. The connector also contains an eight bit data bus, MBD0-MBD7, a mother board interrupt request line, MBIRQ, and 5 lines for power, +5V, and ground.

Address Decoding Circuitry

The interface is memory-mapped to the host computer and responds to READ and WRITE memory activity and not to IN and OUT peripheral commands, used by most peripheral devices.

Memory-mapped Input/Output supports higher-speed data transfer with a wider range of processor instructions. The interface maps into a 128-byte region of memory which may be positioned by the user over the entire 1-megabyte range of system memory. The block always falls, however, at the top of a 4K region. Switch Set S1, containing eight switches, is used to select the mapped region.

The address set on S1 is compared to system address bits A19-A12 by U11, an 8 bit comparator which is gated with AEN to exclude memory addressed during DMA (direct memory access) cycles. AEN is active high during a DMA sequence. When U11 decodes a valid address, pin 19 goes high and is input to U16, an eight input nand. If address bits A11-A7 are also logic high U16 will enable half of U9 (74LS139 dual 2-4 decoder) to decode address bits A6 and A5 to enable a part of the SERIES 500 memory map. The 128-byte memory map is decoded to support the motherboard (IO EN), the interval timers (TIMER), and timer/interrupt support (INTSTUP).

IO EN is an enable signal (active low) which becomes active when the processor is addressing the Series 500 mother board. IO EN is generated through the U11, U16 and U9 address decoding. When doing a write to the mother board, a mono-stable multivibrator (U19) is used to produce a fixed time delay (approximately 250ns) on the WR line. IO EN is used to produce IOSEL when either RD or the fixed delay WR become active low. IOSEL is then inverted and buffered by U12, an octal line driver, to produce MBSEL. MBSEL is an active low signal which is the enable and strobe of the SERIES 500 mother board.

TIMER is an enable signal (active low) which is used to program U13, the programmable interval timer. Details are found in a following section labeled Timer Circuitry.

INTSTUP is an enable signal (active low) that is gated with RD or WR to produce the enable signal to the second half of U9, which is used to decode the four lines used for timer support. These lines are TMR GLOBAL, TMR STATUS, CLR INT, and SET INT.

Timer Circuitry

The programmable interval timer U13 is an Intel 8254 timer containing three programmable 16 bit counters. Each counter is a down-counter with a resolution of one microsecond. The timebase is derived from U1, a 1MHz crystal oscillator.

Each counter can be used independently to count intervals as long as 65,535 microseconds. The counters can be linked, or cascaded (carried), through external circuitry under software control, permitting the measurement of longer intervals. Two linked counters can measure intervals as long as 71 minutes, and three linked counters have a capacity of approximately nine years).

The programmable interval timer also functions as a precision interrupt generator when this mode is selected by software. The TMR GLOBAL location sets an interrupt on/off bit (bit 2), and the cascade on/off bits (bits D0 and D1) in U5 (74LS175 quad D F/F).

U3 is a D-type flip-flop that stores the status of the interrupt. The status is set by latch U5 which contains the interrupt on/off bit. When Counter 0 reaches terminal count (when it counts down to 0), the output line from this counter goes active low. If the interrupt bit is set, U3 will turn on at the Q output, issuing the interrupt selected in U21.

U21 (74LS175 QUAD D F/F) contains the interrupt level selected from software by the SET INT LEVEL Command.

U5 and U3 are reset by the RESET line when the computer is first turned on.

Support Circuitry

U17 and U20 are 74LS645 octal bus transceivers that buffer the processor, interface, and motherboard data busses when the upper address lines A19-A7 decode an access to the SERIES 500. Both are configured to enter a tri-state (high impedance) mode when the processor is addressing a location outside the SERIES 500 memory map.

U18 is a 74LS244 octal buffer which buffers address bits A4-A0, MEMW, and MEMR, from the processor bus.

Wait State Generator

Switch S2 and U10 (74LS165 8 bit shift register) make up a wait state generator which should only be used on computers which do not insert wait states on their system bus. The wait state generator adds an increment of one system clock period to a read or write cycle for each switch closed. With all switches in the off position there are no wait states inserted. Closing switch position 1 adds one wait period, closing position 1 and 2 adds two wait periods and so on, up to a maximum of seven wait periods. U10 does a parallel load of the switch setting when the motherboard is not addressed by the computer. When the motherboard is addressed (MBSEL active) by the computer and Read or Write are asserted U10 leaves the load mode and enters the serial shift mode. The loaded data is shifted, at a clock rate determined by the host computers system clock, to the processors wait state request line IO CHRDY.

The NMI line is a tri-stated line and is enabled to produce an interrupt by U21. The NMI is active only during an interrupt. INT 2, 3, and 5 are activated by U21 and their outputs are controlled by U3, Pin 5 directly.

IBIN-A Specifications

Computers Supported: IBM PC/XT/AT and 100% compatibles IBM PS/2 Model 25, 30, and 100% compatibles.

Power Consumption: IBIN-A: 500mA, 5V DC; IBIN-LP: 150mA, 5V DC.

Address Range: 00F80-FFF80; Switch selectable over range of upper 8 bits (4K byte regions), 128 bytes used. (See manual for valid address table)

Timers: Three 16-bit counters, programmable, cascadable

Resolution: 1µsec

Maximum Count: 89 years

Interrupt Levels: NMI, IRQ2, IRQ3, and IRQ5

Wait States: Switch selectable insertion of wait states.

Example Program

The following QuickBASIC program demonstrates how to load and control the counters on the IBIN-A so that the module may be programmed for a desired time interval. This information is useful for those wishing to write their own low-level drivers for the IBIN-A or IBIN-LP. Programmers who are using KDAC500 or a third party software package need not concern themselves with this example.

```
'*************************************************************************
'* Interval Timing Test for IBIN-A
'*************************************************************************
    CLS
    DEF SEG = &HCFF0

start:
    GOSUB gettime

    high.zero = INT(counter.zero / 256)
    low.zero = counter.zero - (256 * high.zero)

    high.one = INT(counter.one / 256)
    low.one = counter.one - (256 * high.one)

    high.two = INT(counter.two / 256)
    low.two = counter.two - (256 * high.two)

    POKE &HE0, timer.global
    POKE &HC3, 52
    POKE &HC0, low.zero
    POKE &HC0, high.zero
    POKE &HC3, 116
    POKE &HC1, low.one
    POKE &HC1, high.one
    POKE &HC3, 180
    POKE &HC2, low.two
    POKE &HC2, high.two

    '** Read interval timer
```

```
    WHILE INKEY$ = ""
        POKE &HC3, 0
        low.zero = PEEK(&HC0)
        high.zero = PEEK(&HC0)
        counter.zero = low.zero + (high.zero * 256)

        POKE &HC3, 64
        low.one = PEEK(&HC1)
        high.one = PEEK(&HC1)
        counter.one = low.one + (high.one * 256)

        POKE &HC3, 128
        low.two = PEEK(&HC2)
        high.two = PEEK(&HC2)
        counter.two = low.two + (high.two * 256)

        LOCATE 15, 1
        PRINT USING "counter 2 : ######"; counter.two
        PRINT USING "counter 1 : ######"; counter.one
        PRINT USING "counter 0 : ######"; counter.zero
    WEND
    CLS
    GOTO start

'*************************************************************************
'* Subroutine to calculate counts needed for desired interval
'*************************************************************************

gettime:
    INPUT "Enter interval time in seconds ( To 6 decimal places ) => "; sec#
    IF sec# <= .065535 THEN
        timer.global = 0
        Interval = sec# / .000001
        counter.zero = Interval
    END IF

    IF sec# > .065535 AND sec# <= 4294 THEN
        timer.global = 1
        cnt = 65535

        DO
            tim# = sec# / .000001
            remainder# = tim# MOD cnt
            IF remainder# <> 0 THEN cnt = cnt - 1
        LOOP UNTIL remainder# = 0

        counter.one = cnt: counter.zero = tim# \ cnt
    END IF

    IF sec# > 4294 THEN
        timer.global = 3
```

IBIN-A PARTS LIST

Circuit Desig.	Description	Keithley Part No.
	SOCKET, SPRING	SO-83-1
	BRACKET	500-317
	CONNECTOR	CS-490
	CONNECTOR	CS-492
C2-C5, C7-C18,C20	CAPACITORS, 1µF, 20%, 50V, CERAMIC	C-365-.1
C23	CAPACITOR, 10µF, -20 +100%, 25V, ALUM ELEC	C-314-10
C24	CAPACITOR, 100pF, 10%, 1000V, CERAMIC	C-64-100p
C29, C30	CAPACITOR, 270pF, 20%, 100V, CERAMIC/FERRITE	C-386-270p
J2	CONNECTOR, FEMALE 25 PIN	CS-628
R1-R4	THICK FILM (10 PIN, 4.7K)	TF-114-1
R5	RESISTOR, 3.01K, 1%, 1/8W, METAL FILM	R-88-3.01K
R6	RESISTOR, 4.7K, 5%, 1/4W, COMPOSITION OR FILM	R-76-4.7K
S1	SWITCH, SLIDE	SW-449-8
S2	VERTICAL MOUNT DIP SWITCH, SPST	SW-449-7
TP1, TP3	CONNECTOR, TEST POINT	CS-553
U10	INT. CIRCUIT 74LS165	IC-237
U11	INT. CIRCUIT 74LS688	IC-424
U12	INT. CIRCUIT 74LS240	IC-259
U13	INT. CIRCUIT 8254-2	IC-358
U14	INT. CIRCUIT 74LS04	IC-186
U16	INT. CIRCUIT 7430	IC-126
U18	INT. CIRCUIT 74LS244	IC-230
U19	INT. CIRCUIT 74LS121	IC-118
U2	INT. CIRCUIT 74LS08	IC-215
U20, U17	INT. CIRCUIT 74LS645	IC-307
U3	INT. CIRCUIT 74LS08	IC-144
U4, U22	INT. CIRCUIT 72LS74	IC-384
U5, U21	INT. CIRCUIT 74LS175	IC-157
U6	INT. CIRCUIT 74LS02	IC-179
U7	INT. CIRCUIT 74LS05	IC-141
U8	INT. CIRCUIT 74LS367	IC-161
U9	INT. CIRCUIT 74LS139	IC-190
W1, W2	JUMPER, CIRCUIT	J-3
Y1	1MHz CRYSTAL OSC	CR-23

REVISION	ENG.	DATE
RELEASED		12-3-87
REVISED		3-18-88
REVISED		5-5-89
REVISED	QJ	7-10-90

NOTE:
FOR COMPONENT INFORMATION REFER TO BILL OF MATERIAL, (501-969).

MODEL	NEXT ASSEMBLY	QTY.
500		1
USED ON		

E 1:1	TITLE: COMPONENT LAYOUT, IBIN-A BOARD	
	B	NO. 501-150

HOST COMPUTER (IBM OR 100% COMPATIBLE)

UNUSED GATES

KEITHLEY — KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139

TITLE				
SCHEMATIC, 500 IBIN-A				
SIZE	MODEL	NO	ECO	REV
D	500/570	501-156	14117	F
DRAWN	APPROVED	DATE		
CB		4-27-89		

IBIN-LP PARTS LIST

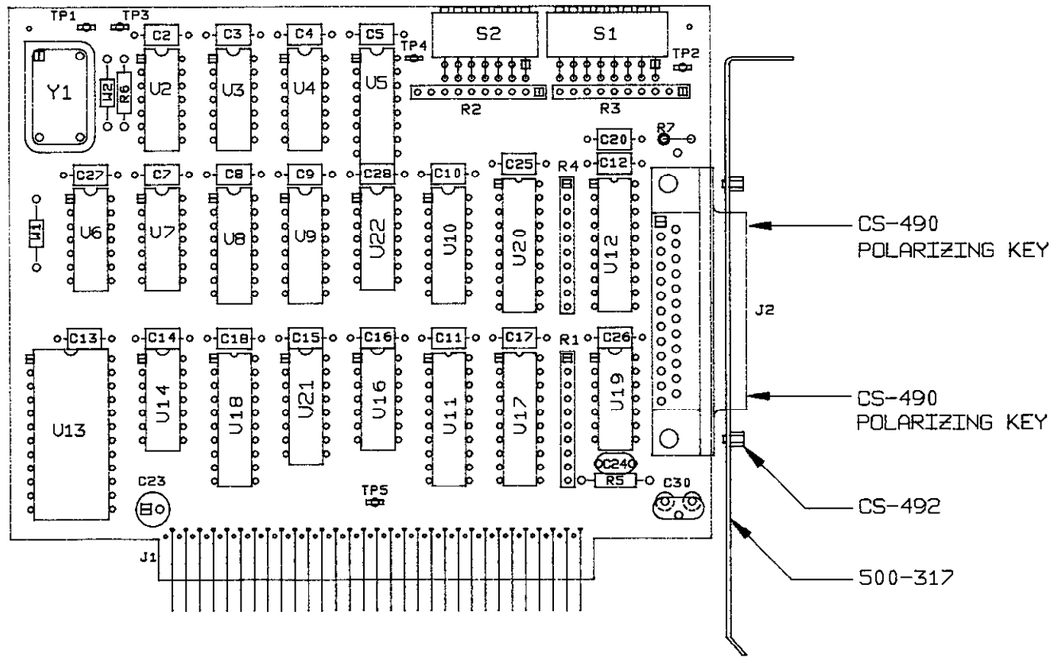
Circuit Desig.	Description	Keithley Part No.
	BRACKET IBM XT	500-317
	CONNECTOR	CS-490
	CONNECTOR	CS-492
	SOCKET, COMPONENT LEAD	SO-83-1
C2	CAP, 1µF,20%,50V,CERAMIC	C-365-.1
C23	CAP,10µF,-20+100%, 25V,ALUM ELEC	C-314-10
C24	CAP, 100PF,10%,1000V,CERAMIC	C-64-100P
C29,30	CAP,270PF,20%,100V,CERAMIC/FERRITE	C-386-270P
C3..5,7..18, 20,25..28	CAP,.1µF,20%,50V,CERAMIC	C-365-.1
J2	CONN,FEMALE 25 PIN	CS-628
R1..4	RES NET,4/7K,2%,1.5W	TF-114-1
R5	RES,3.01K,1%,1/8W,METAL FILM	R-88-3.01K
R6	RES,4.7K,5%,1/4W,COMPOSITION OR FILM	R-76-4.7K
S1	SWITCH,HORIZONTAL MOUNT, DIP, SPST	SW-449-8
S2	HORIZONTAL MOUNT DIP SWITCH, SPST	SW-449-7
TP1,TP3	CONN,TEST POINT	CS-553
U10	IC,8-BIT PARALLEL TO SERIAL,74HCT165	IC-548
U11	IC, 8 BIT MAGNITUDE COMPARATOR	IC-762
U12	IC,INVERTING OCTAL BUFFER,74LS240	IC-259
U13	IC, CMOS PROGRAMMABLE INTERVAL TIMER	IC-764
U14	IC, HEX INVERTER, 74HCT04	IC-444
U16	IC, 8 INPUT NAND GATE	IC-761
U17	IC, OCTAL BUS TRANSCEIVER W 3 STATE O/P	IC-763
U18	IC, OCT BFR/LINE DRIVER/REC,74HCT	IC-483
U19	IC, MONOSTABLE MULTIVIBRATOR, 74LS	IC-118
U2	IC,QUAD 2 INPUT AND GATE,74HCT08	IC-550
U20	IC,OCTAL BUS TRANSCEIVER,74LS645	IC-307
U3	IC,DUAL D FLIP FLOP W/SET & RESE,74HCT74	IC-515
U4,22	IC,QUAD 3 STATE BUFFER	IC-756
U5,21	IC,QUAD D-TYPE FLIP FLOP WITH RESET	IC-757
U6	IC,QUAD 2 INPUT NOR GATE	IC-758
U7	IC,HEX INVERTER W/OPEN DRAIN	IC-759
U8	IC,HEX BUFFER/LINE DRIVER, 3 STATE O/P	IC-760
U9	IC,DUAL 2 TO 4 LINE DECODER,74HCT139	IC-722
W1,2	JUMPER,CIRCUIT	J-3
Y1	OSCILLATOR, 1MHZ	CR-23

HOST COMPUTER (IBM OR 100% COMPATIBLE)

UNUSED GATES

KEITHLEY	KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139
TITLE	SCHEMATIC, 500 IBIN-LP
SIZE	D
MODEL	500/570
NO	501-276
ECO	14559
REV	B
DRAWN	RJS
APPROVED	TML
DATE	9-11-91

LTR.	ECO NO.	REVISION	ENG.	DATE
A	900808	RELEASED	AJS	8-8-90
B	14559	DELETED C29 & C30 AND ADDED R7.		9-11-91



NOTE: FOR COMPONENT INFORMATION REFER TO 500-IBIN-LP PRODUCT STRUCTURE.

NOTE: TP2, TP4, TP5, W2 & C30 NOT INSTALLED.

500		1
MODEL	NEXT ASSEMBLY	QTY.
USED ON		

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 8-8-90	SCALE 1:1	TITLE COMPONENT LAYOUT, IBIN-LP BOARD
KEITHLEY KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139	XX=±.015 ANG.=±1°	DRN. AJS	ENG. APPR. TML	
	XXX=±.005 FRAC.=±1/64	MATERIAL		B NO. 501-270
	SURFACE MAX. 63	FINISH		